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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/776,519	02/12/2004	Jun Miura	TESD.0032	4155

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EXAMINER	
HOANG, ANN THI	
ART UNIT	**PAPER NUMBER**
2836	

DATE MAILED: 06/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/776,519	MIURA, JUN	
	Examiner	Art Unit	
	Ann T. Hoang	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 March 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The objection to the drawings are withdrawn in view of the amendment to the drawings filed 28 March 2006.

Specification

2. The objection to the disclosure is withdrawn in view of the amendment to the specification filed 28 March 2006.

Claim Objections

3. The objection to claim 1 is withdrawn in view of the amended claims filed 28 March 2006.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baek (US 5,073,837) in view of Crompton (US 5,708,574) and Van Ness et al. (US 4,234,920).

Regarding claim 1, Baek discloses a power supply detection circuit provided in an electric device comprising therein a power supply circuit (18); an operating voltage output terminal (10) outputting an operating voltage input from the power supply circuit (18); and a load (20), the power supply detection circuit comprising:

a first circuit provided between the operating voltage output terminal (10) and a power fail terminal (12) for monitoring the operating voltage of the load (20), having one end connected to the operating voltage output terminal (10) and another end connected to the power fail terminal (12) of the load (20), a first switching element (Q2, Q3) controlled to be turned on and off being connected between the one end (10) of the first circuit and the another end (12) of the first circuit; and

a third circuit comprising: a second voltage detection element (ZD2) inputting the voltage output from the operating voltage output terminal (10), and detecting whether the input voltage is a proper voltage or an overvoltage or a reduced voltage; and a third switching element (Q4) controlled to be turned on and off in accordance with detection of the voltage by the second voltage detection element (ZD2), and controlling the first switching element (Q2, Q3) to be turned on and off, wherein

if a proper operating voltage is output from the operating voltage output terminal (10), then the second voltage detection element (ZD2) turns on the third switching element (Q4) to thereby turn on the first switching element (Q2, Q3), whereby the first switching element (Q2, Q3) inputs a voltage signal based on the proper operating voltage to the power fail terminal (12) of the load (20),

if the overvoltage is output from the operating voltage output terminal (10), then

the second voltage detection element (ZD2) turns on the third switching element (Q4) to thereby turn on the first switching element (Q2, Q3), and

if the reduced voltage is output from the operating voltage output terminal (10), then the second voltage detection element (ZD2) fails to turn on the third switching element (Q4) to thereby fail to turn on the first switching element (Q2, Q3), whereby the reduced voltage is prevented from being input to the power fail terminal (12).

If the voltage at operating voltage output terminal (10) is greater than or equal to a predetermined voltage, second voltage detection element (ZD2) senses it as an overvoltage or proper voltage and passes the signal to drive the base of third switching element (Q4), which in turn drives first switching element (Q2, Q3) to be in an ON state so that (Q2, Q3), disclosed as a Darlington pair switching element, may form a signal path from operating voltage output terminal (10) to power fail terminal (12). If the voltage at operating voltage output terminal (10) is less than a predetermined voltage, second voltage detection element (ZD2) acts as an open circuit and cannot turn on third switching element (Q4). With (Q4) in an OFF stage, there is no drive signal for (Q2, Q3) to turn on and (Q2, Q3) fails to establish a signal path between (10) and (12). The power supply detection circuit of Baek serves to open the connection between (10) and (12) upon the occurrence of an undervoltage so that the undervoltage signal is not sent from operating voltage output terminal (10) to power fail terminal (12) when a power fail in the form of an undervoltage is present. See Fig. 2; column 1, lines 7-9; column 2, lines 31-37 and 66-68; column 3, lines 1-13; and column 4, lines 13-33. Baek does not disclose a second circuit for providing overvoltage detection or that the first circuit

monitors the operating voltage of a control microcomputer, as the operating voltage of concern at power fail terminal (12) is of the load (20).

However, Crompton discloses a second circuit comprising: a first voltage detection element (160) inputting a voltage output from an operating voltage output terminal (170) of a power supply, and detecting whether the input voltage is an overvoltage; and a second switching element (175) being connected between operating voltage output terminal (170) and a ground (180), the second switching element (175) is connected between operating voltage output terminal (170) and the ground (180) so as to be controlled to be turned on and off in accordance with detection of the overvoltage by the first voltage detection element (160), wherein

if the overvoltage is output from the operating voltage output terminal (170), the first voltage detection element (160) detects the overvoltage to thereby turn on the second switching element (175), whereby the operating voltage output terminal (170) of the power supply is set at a ground potential.

First voltage detection element (160) is connected to operating voltage output terminal (170) of a power supply so that, if the voltage at (170) exceeds a predetermined value, the voltage will drop across (160) to turn ON second switching element (175) at its base, which pulls operating voltage output terminal (170) to ground (180) as a safety measure. If there is no overvoltage detected at (170), first voltage detection element (160) acts as an open circuit so that second switching element (175) is OFF and does not pull operating voltage output terminal (170) to ground (180). First voltage detection element (160) and second switching element (175) of Crompton are

overvoltage protection devices for operating voltage output terminal (170) of the power supply. See Fig. 3 and column 2, lines 4-12 and 27-38.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the power supply detection circuit of Baek and the overvoltage protection circuit of Crompton and use the overvoltage protection circuit of Crompton to protect the power fail terminal of Baek in order to provide a single protection circuit which offers proper voltage detection and undervoltage detection, as well as overvoltage detection. Such an arrangement would require the second switching element of Crompton to be connected between the power fail terminal of Baek and ground so that, upon the detection of an overvoltage at the operating voltage output terminal by the first voltage detection element, the power fail terminal would be pulled to ground as a safety measure and in order to prevent the overvoltage signal from traveling from the operating voltage output terminal to the power fail terminal. Additionally, the second switching element could only be ON if the first switching element was ON, as this would mean that the voltage at the operating voltage output terminal was greater than the undervoltage threshold value. In the case of undervoltage detection, the first switching element would be OFF and the second switching element would also necessarily be OFF.

Furthermore, Van Ness et al. discloses a power supply detection circuit (22) provided in an electric device comprising therein a power supply circuit (AC, 15, 16); an operating voltage output terminal (17) outputting an operating voltage input from the power supply circuit (AC, 15, 16); and a control microcomputer (12). The power supply

detection circuit (22) is provided between the operating voltage output terminal (17) and a power fail terminal (30) for monitoring the operating voltage of the control microcomputer (12). See abstract; Fig. 1; and column 4, lines 21-33. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the combined power supply detection circuit of Baek in view of Crompton to monitor the operating voltage of a control microcomputer, as Van Ness et al. discloses using a power supply detection circuit to monitor the operating voltage of a control microcomputer, in order to provide reduced voltage and overvoltage protection for the control microcomputer, thereby extending the life of the control microcomputer and the electric device.

Regarding claim 2, Baek discloses that: the first switching element (Q2, Q3) is a first transistor comprising a PNP transistor (Q2), the third switching element (Q4) is a third transistor comprising an NPN transistor,

the second voltage detection element (ZD2) is a second Zener diode having a reverse withstand voltage that would necessarily be slightly lower than the proper operating voltage in order to detect and block undervoltages including those barely under the proper operating voltage,

the first transistor (Q2) is connected so that an emitter terminal is on one end side (10) of a first circuit and so that a collector terminal is on another end side (12) of the first circuit,

a cathode of the second Zener diode (ZD2) is connected to the operating voltage output terminal (10), a base terminal of the third transistor (Q4) is connected to an anode of the second Zener diode (ZD2) through a resistor (R4), and

a collector terminal of the third transistor (Q4) is connected to a base terminal of the first transistor (Q2) through a resistor (R8) and the other transistor (Q3) of the Darlington pair, and an emitter terminal of the third transistor (Q4) is connected to the ground through diodes (ZD3, D3).

See Fig. 2.

Crompton discloses that: the second switching element (175) is a second transistor comprising an NPN transistor,

the first voltage detection element (160) is a first Zener diode having a reverse withstand voltage that would necessarily be slightly higher than the proper operating voltage in order to detect and pass overvoltages including those barely over the proper operating voltage, and

a cathode of the first Zener diode (160) is connected to the operating voltage output terminal (170), an emitter terminal of the second transistor (175) is connected to the ground (180), and a base terminal of the second transistor (175) is connected to an anode of the first Zener diode (160).

See Fig. 3. In order for second transistor (175) to pull the power fail terminal to ground in the event of an overvoltage, as mentioned above, the collector terminal of second transistor (175) would necessarily be connected to the power fail terminal so

that the current could flow from the power fail terminal to ground during the ON state of second transistor (175).

Regarding claims 3 and 5, Baek discloses a constant voltage maintaining circuit (22), provided on the another end of the first circuit connected to the power fail terminal (12), for setting the voltage input to the power fail terminal to be equal to or lower than a constant voltage. See Fig. 2 and column 2, lines 56-62.

6. Claims 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baek (US 5,073,837) in view of Crompton (US 5,708,574) and Van Ness et al. (US 4,234,920), as applied to claims 3 and 5 above, and further in view of the acknowledged prior art.

Regarding both claims 4 and 6, Baek discloses a constant voltage maintaining circuit (22) but not the details of the circuit. However, the acknowledged prior art of Applicant's disclosure discloses a constant voltage maintaining circuit comprising a third Zener diode (53) having a cathode connected to a power fail terminal (56a) and an anode connected to the ground, wherein if a voltage exceeding the reverse withstand voltage of third Zener diode (53) is applied to the third Zener diode (53) in a reverse direction, the third Zener diode (53), a resistance (57) connected between an operating voltage output terminal (58) and the power fail terminal (56a), and a resistance (54) connected to the third Zener diode (53) in parallel maintain the power fail terminal (56a) of the first circuit at the reverse withstand voltage of third Zener diode (53).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the constant voltage maintaining circuit of the acknowledged prior art

as the constant voltage maintaining circuit of Baek in order to provide means of preventing the power fail terminal from rising above a predetermined voltage through cheap electrical components, and in order to provide further overvoltage protection to the power fail terminal in addition to that provided by the second circuit of Crompton. Further, it would have been obvious to one of ordinary skill in the art at the time of the invention to choose the third Zener diode to have a reverse withstand voltage slightly higher than the voltage corresponding to the proper operating voltage of the power fail terminal in order to provide protection against overvoltages, not to exclude voltages barely greater than the proper operating voltage, as those may damage the load.

Response to Arguments

7. Applicant's arguments, see page 10, filed 28 March 2006, with respect to the rejection(s) of claim(s) 1-6 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of a newly found prior art reference that discloses the use of a power supply detection circuit for monitoring the operating voltage of a control microcomputer. One of ordinary skill in the art at the time of the invention would have been motivated to combine a circuit providing reduced voltage protection with a circuit providing overvoltage protection in order to provide both kinds of protection, and to use the reduced voltage and overvoltage protection to monitor the operating voltage of a control microcomputer in order to provide reduced

voltage and overvoltage protection for the control microcomputer, thereby extending the life of the control microcomputer and the electric device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ann T. Hoang, whose telephone number is 571-272-2724. The examiner can normally be reached Mondays through Fridays, 8:00 a.m. to 5:00 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus, can be reached at 571-272-2800 x36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Stephen W Jackson
6-20-06

ATH
19 June 2006

STEPHEN W. JACKSON
PRIMARY EXAMINER